CLAIMS:

What is claimed is:

1. A method operative in an input/output device associated with a computer system, comprising:

performing a plurality of direct memory access transfers with respect to memory of the computer system, wherein parameters of the direct memory access transfers are varied pseudo-randomly.

2. The method of claim 1, wherein the parameters include start address alignment.

3. The method of claim 1, wherein the parameters include transfer size.

4. The method of claim 1, wherein the parameters include at least one of transfer width and byte lane enables.

5. The method of claim 1, wherein the parameters include at least one of request assertion time, request deassertion time, number of wait states, number of idle states, disconnect count, retry limit, and whether to override a latency timer.

6. The method of claim 1, further including performing additional bus commands.

7. The method of claim 6, wherein the additional bus commands include all possible bus commands.

8. The method of claim 1, wherein the direct memory transfers are performed concurrently with memory accesses by a processor in the computer system.

9. The method of claim 8, wherein the processor and the input/output device access memory locations within a same block of memory.

10. The method of claim 8, wherein the processor and the input/output device access a same memory location.

11. The method of claim 1, wherein the memory includes cache memory.

12. A computer program product in a computer readable medium and operative in an input/output device associated with a computer system, comprising functional descriptive material that when processed by an input/output device, enables the input/output device to perform acts of:

performing a plurality of direct memory access transfers with respect to memory of the computer system, wherein parameters of the direct memory access transfers are varied pseudo-randomly.

13. The computer program product of claim 12, wherein the parameters include start address alignment.

14. The computer program product of claim 12, wherein the parameters include transfer size.

15. The computer program product of claim 12, wherein the parameters include at least one of transfer width and byte lane enables.

16. The computer program product of claim 12, wherein the parameters include at least one of request assertion time, request deassertion time, number of wait states, number of idle states, disconnect count, retry limit, and whether to override a latency timer.

17. The computer program product of claim 12, wherein the functional descriptive material enables the computer to perform additional acts including performing additional bus commands.

18. The computer program product of claim 17, wherein the additional bus commands include all possible bus commands.

19. The computer program product of claim 12, wherein the direct memory transfers are performed concurrently with memory accesses by a processor in the computer system.

20. The computer program product of claim 19, wherein the processor and the input/output device access memory locations within a same block of memory.

21. The computer program product of claim 19, wherein the processor and the input/output device access a same memory location.

22. The computer program product of claim 12, wherein the memory includes cache memory.

23. A computer program product in a computer readable medium comprising functional descriptive material that when processed by an input/output device, enables the input/output device to perform acts of:

directing the at least one peripheral device to perform direct memory access transfers with respect to the memory and with pseudo-random variations in direct memory access transfer parameters;

accessing a portion of the memory concurrently with the at least one peripheral device.

24. An input/output device comprising means for:

performing a plurality of direct memory access transfers with respect to memory of a computer system, wherein parameters of the direct memory access transfers are varied pseudo-randomly.

25. The input/output device of claim 24, wherein the parameters include start address alignment.

26. The input/output device of claim 24, wherein the parameters include transfer size.

27. The input/output device of claim 24, wherein the parameters include at least one of transfer width and byte lane enables.

28. The input/output device of claim 24, wherein the parameters include at least one of request assertion

time, request deassertion time, number of wait states, number of idle states, disconnect count, retry limit, and whether to override a latency timer.

29. The input/output device of claim 24, further comprising means for performing additional bus commands.

30. The input/output device of claim 29, wherein the additional bus commands include all possible bus commands.

31. The input/output device of claim 24, wherein the direct memory transfers are performed concurrently with memory accesses by a processor in the computer system.

32. The input/output device of claim 31, wherein the processor and the input/output device access memory locations within a same block of memory.

33. The input/output device of claim 31, wherein the processor and the input/output device access a same memory location.

34. The input/output device of claim 24, wherein the memory includes cache memory.

35. A computer system comprising:

memory;

at least one peripheral device configured to be able to access the memory;

at least one processor associated with the memory; and

functional descriptive material within the memory, wherein the at least one processor processes the functional descriptive material to perform acts of:

directing the at least one peripheral device to perform direct memory access transfers with respect to the memory and with pseudo-random variations in direct memory access transfer parameters; and

accessing a portion of the memory concurrently with the at least one peripheral device.

36. The computer system of claim 35, further comprising a test nanokernel in the memory, wherein the at least one processor executes the test nanokernel to enable processing of the functional descriptive material.